IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/765,510
Priority Filing Date ..... January 19, 2001
Inventor ..... Kunal R. Parekh et al.
Assignee ..... Micron Technology, Inc.
Priority Group Art Unit 2813
Priority Examiner ..... Y. Huynh
Attorney's Docket No. MI22-1816
Title: Capacitors, DRAM Arrays, Monolithic Integrated Circuits, And Methods of Forming Capacitors, DRAM Arrays, And Monolithic Integrated Circuits

PRELIMINARY AMENDMENT

To: Assistant Commissioner for Patents
Washington, D.C. 20231

From: Frederick M. Fliegel, Ph.D.
(Tel. 509-624-4276; Fax 509-838-3424)
Wells, St. John, Roberts, Gregory & Matkin P.S.
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Sir:

This is a preliminary amendment accompanying a Request for Continuation Application for the above-entitled patent application. Prior to examining the application, please enter the following amendments.

AMENDMENTS

In the Specification

At page 1, after the title insert:

CROSS REFERENCE TO RELATED APPLICATION

This patent application is a Continuation Application of U.S. Patent Application Serial No. 09/765,510, filed on January 19, 2001, entitled "Capacitors, DRAM Arrays, Monolithic Integrated Circuits, And Methods of Forming Capacitors, DRAM Arrays, And Monolithic Integrated Circuits", naming Kunal R. Parekh, John K. Zahurak and Phillip G. Wald as inventors, which is a Continuation Application of U.S. Patent Application Serial No. 08/887,742, filed on July 3, 1997, now U.S. Patent No. 6,207,523.

In the Claims

1. (Amended) A method of forming a capacitor comprising the following steps:

forming a capacitor plate, forming a capacitor plate comprising:

forming a solid mass of silicon material within an opening formed over a doped region of a silicon substrate, the mass comprising two forms of silicon, the mass including undoped silicon in physical contact with the doped region; and

substantially selectively forming rugged polysilicon from one of the forms of silicon and not from another of the forms of silicon; and

forming a cell plate proximate the rugged polysilicon.

2. The method of claim 1 wherein the two forms of silicon comprise doped silicon and undoped silicon.

3. The method of claim 2 wherein the doped silicon comprises a dopant concentration of at least 5×10^{18} atoms/cm^3 and wherein the undoped silicon comprises a dopant concentration of less than 5×10^{18} atoms/cm^3.

4. The method of claim 2 wherein the doped silicon comprises a dopant concentration of at least 1×10^{19} atoms/cm^3 and wherein the undoped silicon comprises a dopant concentration of less than or equal to 1×10^{18} atoms/cm^3.

5. (Amended) A method of forming a capacitor comprising the following steps:

forming a solid mass of silicon material over a doped region of a silicon substrate, the mass comprising exposed doped silicon and exposed undoped silicon, and including undoped silicon in contact with the doped region;

substantially selectively forming rugged polysilicon from the exposed undoped silicon and not from the exposed doped silicon; and

forming a cell plate proximate the rugged polysilicon.

6. The method of claim 5 wherein the step of forming a mass of silicon material comprises forming a layer of doped silicon between two layers of undoped silicon.

7. (Amended) The method of claim 5, further comprising conductively doping the undoped silicon after forming the rugged polysilicon.

8. (Amended) The method of claim 5, further comprising, after forming the rugged polysilicon, out-diffusing impurity from the doped silicon into the undoped silicon to conductively dope the undoped silicon.

9. The method of claim 5 wherein the step of forming the mass comprises forming the exposed undoped silicon to be substantially amorphous.

10. The method of claim 5 wherein the step of forming the mass comprises forming the exposed doped silicon to be substantially polycrystalline.

11. (Amended) A method of forming a capacitor comprising the following steps:

forming an insulative layer over a doped region of a semiconductor substrate;

forming an opening through the insulative layer to the doped region

forming two forms of silicon within the opening, the two forms of silicon including undoped silicon in contact with the doped region

exposing the two forms of silicon to common subsequent processing conditions which substantially selectively form rugged polysilicon from one of the exposed two forms of silicon and not from another of the exposed two forms of silicon; and

forming a cell plate proximate the storage node.

12. The method of claim 11 wherein the two forms of silicon comprise doped silicon and undoped silicon.

13. (Amended) A method of forming a capacitor comprising the following steps:

forming an insulative layer over a doped region on a semiconductor substrate;

forming an opening through the insulative layer to the doped region;

forming silicon material within the opening, the silicon material comprising doped silicon and undoped silicon and defining a capacitor storage node, a portion of the undoped silicon being in physical contact with the doped region;

removing a portion of the insulative layer to expose a sidewall surface of the storage node, the exposed sidewall surface comprising undoped silicon;

forming HSG from the undoped silicon of the exposed sidewall surface; and

forming a cell plate proximate the storage node.

14. The method of claim 13 wherein the doped silicon comprises polysilicon and the undoped silicon comprises substantially amorphous silicon.

15. The method of claim 13 wherein the step of forming the silicon material comprises forming a layer of doped silicon between two layers of undoped silicon.

16. The method of claim 13 wherein the step of forming the silicon material comprises forming a layer of doped polysilicon between two layers of undoped substantially amorphous silicon.

17. (Amended) A method of forming a capacitor comprising the following steps:

forming an insulative layer over a doped region on a semiconductor substrate;

forming an opening through the insulative layer to the doped region;

forming an undoped silicon layer within the opening to narrow the opening, a portion of the undoped silicon contacting the doped region;

forming a doped silicon layer within the narrowed opening, the undoped silicon layer and doped silicon layer together defining a capacitor storage node; and

forming a cell plate proximate the storage node.

18. The method of claim 17 wherein the undoped silicon layer comprises substantially amorphous silicon.

19. The method of claim 17 wherein the doped silicon layer comprises polysilicon.

20. The method of claim 17 further comprising:

removing a portion of the insulative layer to expose a sidewall surface of the storage node comprising the undoped silicon layer; and

forming rugged polysilicon from the exposed sidewall surface.

21. The method of claim 17 further comprising:

exposing a surface of the capacitor storage node comprising undoped silicon;

exposing a surface of the capacitor storage node comprising doped silicon; and

substantially selectively forming HSG polysilicon from the exposed capacitor storage node surface comprising undoped silicon and not from the exposed capacitor storage node surface comprising doped silicon.

22. The method of claim 21 wherein the formation of the rugged polysilicon comprises:

in situ HF cleaning of the exposed sidewall surface;

seeding the exposed sidewall surface with polysilicon; and

annealing the seeded sidewall surface at about 560□ C for about 20 minutes.

23. The method of claim 21 wherein the formation of the rugged polysilicon comprises:

in situ HF cleaning of the exposed sidewall surface;

seeding the exposed sidewall surface with polysilicon;

annealing the seeded sidewall surface at about 560□ C for about 20 minutes; and

a polysilicon etch after the annealing to remove any monolayers of silicon.

24. (Amended) A method of forming a capacitor comprising the following steps:

forming an insulative layer over a doped region on a semiconductor substrate;

forming an opening through the insulative layer to the doped region;

forming a first undoped silicon layer within the opening to narrow the opening, a portion of the undoped silicon layer contacting the doped region;

forming a doped silicon layer within the narrowed opening to further narrow the opening;

forming a second undoped silicon layer within the further narrowed opening; the first undoped silicon layer, second undoped silicon layer and doped silicon layer together defining a capacitor storage node;

removing a portion of the insulative layer to expose a sidewall surface of the storage node comprising the first undoped silicon layer;

forming rugged polysilicon on the exposed sidewall surface; and

forming a cell plate proximate the storage node.

25. The method of claim 24 further comprising:

exposing a surface of the capacitor storage node comprising the second undoped silicon layer;

exposing a surface of the capacitor storage node comprising the doped silicon layer; and

substantially selectively forming HSG polysilicon from the exposed capacitor storage node surface comprising undoped silicon and not from the exposed capacitor storage node surface comprising doped silicon.

Cancel claims 26-43.

New Claims

44. The method of claim 1, wherein forming a cell plate comprises forming a capacitor dielectric layer and a complementary capacitor plate proximate the rugged polysilicon.

45. The method of claim 5, wherein forming a cell plate comprises forming a capacitor dielectric layer and a complementary capacitor plate proximate the rugged polysilicon and doped silicon.

46. The method of claim 11, wherein forming a cell plate comprises:

forming a dielectric layer proximate the storage node; and

forming a cell plate layer proximate the dielectric layer.

47. The method of claim 13, wherein forming a cell plate comprises:

forming a capacitor dielectric layer proximate the storage node; and

forming a complementary capacitor plate proximate the capacitor dielectric layer.

48. The method of claim 17, wherein forming a cell plate comprises:

forming a capacitor dielectric layer proximate the storage node; and

forming a complementary capacitor plate proximate the capacitor dielectric layer.

49. The method of claim 24, wherein forming a cell plate comprises:

forming a dielectric layer proximate the storage node; and

forming a cell plate layer proximate the dielectric layer.

50. A method of forming a capacitor comprising:

forming an insulative layer over a doped region formed on a semiconductor substrate;

forming an opening through the insulative layer to the doped region;

filling the opening with silicon material, the silicon material comprising doped silicon and undoped silicon and defining a capacitor storage node;

removing a portion of the insulative layer to expose a sidewall surface of the storage node, the exposed sidewall surface comprising undoped silicon;

forming HSG from the undoped silicon of the exposed sidewall surface; and

forming a cell plate proximate the storage node.

51. The method of claim 50, wherein forming a cell plate comprises:

forming a capacitor dielectric layer proximate the storage node; and

forming a complementary capacitor plate proximate the capacitor dielectric layer.

52. The method of claim 50 wherein the doped silicon comprises polysilicon and the undoped silicon comprises substantially amorphous silicon.

53. The method of claim 50 wherein forming the silicon material comprises forming a layer of doped silicon inside a layer of undoped silicon.

54. The method of claim 50 wherein filling the opening with silicon material comprises forming a layer of doped polysilicon within a layer of undoped substantially amorphous silicon.

55. A method of forming a capacitor comprising:

forming an insulative layer over a doped region formed on a semiconductor substrate;

forming an opening through the insulative layer to the doped region;

forming an undoped silicon layer within the opening to narrow the opening;

filling the narrowed opening with a doped silicon layer, the undoped silicon layer and doped silicon layer together defining a capacitor storage node; and

forming a cell plate proximate the storage node.

56. The method of claim 55, wherein forming a cell plate comprises

forming a capacitor dielectric layer proximate the storage node; and

forming a complementary capacitor plate proximate the capacitor dielectric layer.

57. The method of claim 55 further comprising:

exposing a surface of the capacitor storage node comprising undoped silicon;

exposing a surface of the capacitor storage node comprising doped silicon; and

substantially selectively forming HSG polysilicon from the exposed capacitor storage node surface comprising undoped silicon and not from the exposed capacitor storage node surface comprising doped silicon.

58. The method of claim 57 wherein forming HSG polysilicon comprises:

in situ HF cleaning of exposed doped and undoped silicon surfaces;

seeding the exposed undoped silicon surface with polysilicon; and

annealing the seeded surface at about 560 ° C for about 20 minutes.

59. The method of claim 57 wherein forming HSG polysilicon comprises:

in situ HF cleaning of the exposed doped and undoped silicon surfaces;

seeding the exposed undoped silicon surface with polysilicon;

annealing the seeded surface at about 560° C for about 20 minutes; and

a polysilicon etch after the annealing to remove any monolayers of silicon.

REMARKS

Claims 1, 5, 7, 8, 11, 13, 17 and 24 have been amended, claims 26-43 have been canceled and new claims 44-59 have been added. Claims 1-25 and 44-59 are now pending in the application.

The amendments to the claims, and new claims 44-59, are supported at least by page 6, line 8 through page 18, line 19 of the application as originally filed. No new matter is added by the amendments to the claims or by new claims 44-59. New claims 44-59 distinguish over the art of record and are allowable.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page(s) are captioned "**Version with markings to show changes made**."

This application is believed to be in condition for allowance and action to that end is requested. The Examiner is requested to telephone the undersigned in the event that the next office action is one other than a Notice of Allowance. The undersigned is available during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: Sept. 18, 2001

By: _____
Frederick M. Fliegel, Ph.D.
Reg. No. 36,138

Version with markings to show changes made

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/765,510
Priority Filing Date ..... January 19, 2001
Inventor ..... Kunal R. Parekh et al.
Assignee ..... Micron Technology, Inc.
Priority Group Art Unit 2813
Priority Examiner ..... Y. Huynh
Attorney's Docket No. MI22-1816
Title: Capacitors, DRAM Arrays, Monolithic Integrated Circuits, And Methods of Forming Capacitors, DRAM Arrays, And Monolithic Integrated Circuits

37 CFR §1.121(b)(1)(iii) AND 37 CFR §1.121(c)(1)(ii) FILING REQUIREMENTS TO ACCOMPANY PRELIMINARY AMENDMENT

Deletions are bracketed, additions are underlined.

In the Specification

The following paragraph was inserted at page 1, after the title:

CROSS REFERENCE TO RELATED APPLICATION

This patent application is a Continuation Application of U.S. Patent Application Serial No. 09/765,510, filed on January 19, 2001, entitled "Capacitors, DRAM Arrays, Monolithic Integrated Circuits, And Methods of Forming Capacitors, DRAM Arrays, And Monolithic Integrated Circuits", naming Kunal R. Parekh, John K. Zahurak and Phillip G. Wald as inventors, which is a Continuation Application of U.S. Patent Application Serial No. 08/887,742, filed on July 3, 1997, now U.S. Patent No. 6,207,523.

In the Claims

1. (Amended) A method of forming a capacitor comprising the following steps:

forming a capacitor plate, forming a capacitor plate comprising:

forming a solid mass of silicon material within an opening formed over a [node location] doped region of a silicon substrate, the mass comprising two forms of silicon, the mass including undoped silicon in physical contact with the doped region; and

substantially selectively forming rugged polysilicon from one of the forms of silicon and not from [the other] another of the forms of silicon; and

forming a cell plate proximate the rugged polysilicon.

[forming a capacitor dielectric layer and a complementary capacitor plate proximate the rugged polysilicon.]

5. (Amended) A method of forming a capacitor comprising the following steps:

forming a solid mass of silicon material over a [node location] doped region of a silicon substrate, the mass comprising exposed doped silicon and exposed undoped silicon, and including undoped silicon in contact with the doped region;

substantially selectively forming rugged polysilicon from the exposed undoped silicon and not from the exposed doped silicon; and

forming a cell plate proximate the rugged polysilicon.

[forming a capacitor dielectric layer and a complementary capacitor plate proximate the rugged polysilicon and doped silicon.]

7. (Amended) The method of claim 5, further comprising conductively doping the undoped silicon after forming the rugged polysilicon.

8. (Amended) The method of claim 5, further comprising, after forming the rugged polysilicon, out-diffusing impurity from the doped silicon into the undoped silicon to conductively dope the undoped silicon.

11. (Amended) A method of forming a capacitor comprising the following steps:

forming an insulative layer over a [node location] doped region of a semiconductor substrate;

forming an opening through the insulative layer to the [node location] doped region

forming two forms of silicon within the opening, [the two forms of silicon together forming a capacitor storage node] the two forms of silicon including undoped silicon in contact with the doped region

exposing the two forms of silicon to common subsequent processing conditions which substantially selectively [forming] form rugged polysilicon from one of the exposed two forms of silicon and not from [the other] another of the exposed two forms of silicon; and

forming a cell plate proximate the storage node.

[forming a dielectric layer proximate the storage node; and

forming a cell plate layer proximate the dielectric layer.]

13. (Amended) A method of forming a capacitor comprising the following steps:

forming an insulative layer over a [node location] doped region on a semiconductor substrate;

forming an opening through the insulative layer to the [node location] doped region;

forming silicon material within the opening, the silicon material comprising doped silicon and undoped silicon and defining a capacitor storage node, a portion of the undoped silicon being in physical contact with the doped region;

removing a portion of the insulative layer to expose a sidewall surface of the storage node, the exposed sidewall surface comprising undoped silicon;

forming HSG from the undoped silicon of the exposed sidewall surface; and

forming a cell plate proximate the storage node.

[forming a capacitor dielectric layer proximate the storage node; and

forming a complementary capacitor plate proximate the capacitor dielectric layer.]

17. (Amended) A method of forming a capacitor comprising the following steps:

forming an insulative layer over a [node location] doped region on a semiconductor substrate;

forming an opening through the insulative layer to the [node location] doped region;

forming an undoped silicon layer within the opening to narrow the opening, a portion of the undoped silicon contacting the doped region;

forming a doped silicon layer within the narrowed opening, the undoped silicon layer and doped silicon layer together defining a capacitor storage node; and

forming a cell plate proximate the storage node.

[forming a capacitor dielectric layer proximate the storage node; and

forming a complementary capacitor plate proximate the capacitor dielectric layer.]

24. (Amended) A method of forming a capacitor comprising the following steps:

forming an insulative layer over a [node location] doped region on a semiconductor substrate;

forming an opening through the insulative layer to the [node location] doped region;

forming a first undoped silicon layer within the opening to narrow the opening, a portion of the undoped silicon layer contacting the doped region;

forming a doped silicon layer within the narrowed opening to further narrow the opening;

forming a second undoped silicon layer within the further narrowed opening; the first undoped silicon layer, second undoped silicon layer and doped silicon layer together defining a capacitor storage node;

removing a portion of the insulative layer to expose a sidewall surface of the storage node comprising the first undoped silicon layer;

forming rugged polysilicon on the exposed sidewall surface; and

forming a cell plate proximate the storage node.

[forming a dielectric layer proximate the storage node; and

forming a cell plate layer proximate the dielectric layer.]

Claims 26-43 have been canceled and claims 44-59 have been added.

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